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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,634	08/04/2003	Christopher L. Hamlin	03-0339	7201

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EXAMINER	
LEVIN, NAUM B	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,634	HAMLIN, CHRISTOPHER L.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application 10/634,634 and Amendment filed on 05/27/2005. Claims 1-45 remain pending in the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

1. Claims 1, 13, 25 and 37 rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 1, 13, 25 and 37 fail to correspond in scope with that which applicant regard as the invention can be found in the reply filed 05/27/05. In that paper, applicant has stated:

"Independent claim 1 recites an element of "slice". As indicated in Specification,

A slice is a pre-manufactured chip in which all silicon layers have been built ... (page 6, paragraph [0016]),

A slice is a constrained specification. A slice is an abstract specification of all IP, characteristics of interconnect, memory structures, I/O's, a transistor array, embedded programmable logic (if there is any), and the like ... (page 7, paragraph [0019])".

This statement indicates that the invention is different from what is defined in the claim(s) because Applicant provide in Specification at least three different definitions of "slice":

A. a slice is a pre-manufactured chip,

B. a slice is constrained specification, and

C. a slice is an abstract specification.

Thereby the specification does not conclude with claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim Objections

2. Claim 37 is objected to because following informalities:

replace "two mapping" with – two mappings--.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5-15, 17-27 and 29-45 are rejected under 35 U.S.C. 102(b) as being unpatentable by Lee et al. (US Patent 5,500,805).

As to claims 1, 13, 25 and 37 Lee discloses:

(1) A method for mapping platform-based (array based) design to multiple foundry processes, comprising (col.1, ll.14-17):

(a) predefining a slice (library 509/masterslises/specification) (col.12, ll.62-63; col.13, ll.7-24);

(b) mapping (adapting/adjusting) said slice onto a first fabrication process with a first set of design rules (specific fabrication process of a given vendor, including its

specific performance parameters) to produce a first result (col.12, ll.42-49; col.12, ll.56-58);

(c) evaluating (analyzing) said slice with a second fabrication process with a second set of design rules to produce a second result (col.6, ll.44-61; col.7, ll.45-67; col.8, ll.1-67; col.9, ll.1-38); and

(d) comparing said first result and said second result to produce a third result (col.3, ll.63-67; col.4, ll.1-32; col.9, ll.39-67; col.10, ll.1-7; col.12, ll.64-67; col.13, ll.1-6);

(13) An apparatus (computer) for mapping platform-based (array based) design to multiple foundry processes, comprising (col.1, ll.14-17; col.1, ll.28-59):

(a) predefining a slice (library 509/masterslises/specification) (col.12, ll.62-63; col.13, ll.7-24);

(b) mapping (adapting/adjusting) said slice onto a first fabrication process with a first set of design rules (specific fabrication process of a given vendor, including its specific performance parameters) to produce a first result (col.12, ll.42-49; col.12, ll.56-58);

(c) evaluating (analyzing) said slice with a second fabrication process with a second set of design rules to produce a second result (col.6, ll.44-61; col.7, ll.45-67; col.8, ll.1-67; col.9, ll.1-38); and

(d) comparing said first result and said second result to produce a third result (col.3, ll.63-67; col.4, ll.1-32; col.9, ll.39-67; col.10, ll.1-7; col.12, ll.64-67; col.13, ll.1-6);

(25) A computer-readable medium having computer-executable instructions for performing a method for mapping platform-based (array based) design to multiple foundry processes, comprising (col.1, ll.14-17; col.1, ll.28-59):

(a) predefining a slice (library 509/masterslises/specification) (col.12, ll.62-63; col.13, ll.7-24);

(b) mapping (adapting/adjusting) said slice onto a first fabrication process with a first set of design rules (specific fabrication process of a given vendor, including its specific performance parameters) to produce a first result (col.12, ll.42-49; col.12, ll.56-58);

(c) evaluating (analyzing) said slice with a second fabrication process with a second set of design rules to produce a second result (col.6, ll.44-61; col.7, ll.45-67; col.8, ll.1-67; col.9, ll.1-38); and

(d) comparing said first result and said second result to produce a third result (col.3, ll.63-67; col.4, ll.1-32; col.9, ll.39-67; col.10, ll.1-7; col.12, ll.64-67; col.13, ll.1-6);

(37) A computer-readable medium having stored thereon a database (library) having a data structure, said data structure comprising: (col.1, ll.14-17; col.1, ll.28-59):

(a) a first field containing data representing a slice definition (library 509/master slices/specification) (col.12, ll.62-63; col.13, ll.7-24);

(b) a second field containing data representing a first set of design rules (specific fabrication process of a given vendor, including its specific performance parameters) with which said slice definition is mapped (adapting/adjusting) to a first fabrication process (col.12, ll.42-49; col.12, ll.56-58);

(c) a third field containing data representing a second set of design rules with which said slice definition is mapped (adapting/adjusting) to a second fabrication process (col.6, ll.44-61; col.7, ll.45-67; col.8, ll.1-67; col.9, ll.1-38); and

(d) a fourth field containing data representing a result of computed comparison between results of said two mappings (col.3, ll.63-67; col.4, ll.1-32; col.9, ll.39-67; col.10, ll.1-7; col.12, ll.64-67; col.13, ll.1-6).

As to claims 2-3, 5-12, 14-15, 17-24, 26-27, 29-36 and 38-45 Lee recites:

(2), (14), (26), (38) The method/apparatus/program/database, wherein said slice is a Rapidslice (instance of pre-manufactured chip/masterslice of gate arrays) (col.4, ll.60-62; col.5, ll.24-51; col.12, ll.62-63; col.13, ll.7-24);

(3), (15), (27) The method/apparatus/program, wherein said step (d) is a hybrid analysis whereby evaluation of an element of said slice is discontinued when said element is established to be accessible in said second fabrication process (col.6, ll.24-61);

(5), (17), (29), (39) The method/apparatus/program/database, wherein said third result including at least one variable that is invariant in said platform-based design (col.5, ll.52-67; col.6, ll.1-10; col.7, ll.27-44);

(6), (18), (30), (40) The method/apparatus/program/database, further comprising modifying said slice definition based on said third result (col.13, ll.7-24);

(7), (19), (31), (41) The method/apparatus/program/database, further comprising optimizing a metallization process giving a final function of said slice based on said third result (col.12, ll.62-67; col.13, ll.1-6);

(8), (20), (32), (42) The method/apparatus/program/database, further comprising modifying said first fabrication process based on said third result (col.4, ll.60-62; col.12, ll.42-49; col.12, ll.56-58);

(9), (21), (33), (43) The method/apparatus/program/database, further comprising modifying said second fabrication process based on said third result (col.4, ll.60-62; col.6, ll.44-61; col.7, ll.45-67; col.8, ll.1-67; col.9, ll.1-38);

(10), (22), (34) The method/apparatus/program, further comprising storing said third result into a database (col.1, ll.28-39; col.5, ll.24-51; col.13, ll.7-24);

(11), (23), (35), (44) The method/apparatus/program/database, further comprising optimizing platform architecture used to predefine said slice based on said third result (col.6, ll.11-23);

(12), (24), (36), (45) The method/apparatus/program/database, further comprising optimizing temporal structure of interconnect of said platform architecture based on said third result (col.6, ll.11-23).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 16 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Chen et al. (US Patent 6,757,882).

With respect to claims 4, 16 and 28 Lee teaches the features above but lacks a method/apparatus/program for mapping platform-based (array based) design to multiple foundry processes, wherein comparing said first result and said second result to produce a third result is accomplished with a network-distributed processing system.

As to claims 4, 16 and 28 Chen discloses:

The method/apparatus/program, wherein said step (d) is accomplished with a network-distributed processing system (col.3, ll.28-39; col.17, ll.18-61).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Chen's teaching regarding the method/apparatus/program for mapping platform-based (array based) design to multiple foundry processes, wherein comparing said first result and said second result to produce a third result is accomplished with a network-distributed processing system and use it in Lee's invention to improve a communication speed between customer/designer and plurality of separate fabrication facilities and processes of plurality of vendors, thereby increasing a speed of method and apparatus for mapping platform-based (array based) design to multiple foundry processes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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AU-2825